IN THE SPECIFICATION:

Please insert the following heading and sentence, prior to the heading reading "BACKGROUND OF THE INVENTION" on page 1 of the application:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This is a division of Application No. 09/286,168, filed on April 5, 1999.--

Please amend the paragraph beginning at line 27 on page 2 of the application as follows:

--The present invention provides a trench metal oxide semiconductor field effect transistor (MOSFET) with a rugged gate dielectric layer which exhibits lower gate leakage current. Gate dielectric (e.g. oxide) is grown on the trench walls and bottom at a temperature sufficiently high to reduce the viscosity of the oxide during growth to result in an oxide layer of more uniform thickness. In one embodiment, the high-temperature oxide layer is grown at 1,100°C to a thickness of about 500 Å thick and exhibits reduced gate leakage current and higher gate rupture voltage compared to a trench transistor with a gate oxide layer of similar thickness grown at the lower temperatures (e.g., 950°C) conventionally used in the industry. In a preferred embodiment, a gate dielectric layer is made from a first layer of high-temperature gate oxide, a layer of silicon nitride, and a second layer of gate oxide. This composite gate dielectric layer at optimized thicknesses results in even lower gate leakage current and higher gate rupture voltage.--

Please amend the paragraph beginning at line 18 on page 3 of the application as follows:

-- In another embodiment, the present invention provides a field effect transistor formed on a silicon substrate, the transistor including a trench extending into the substrate, the trench being substantially filled by a conductive material that is